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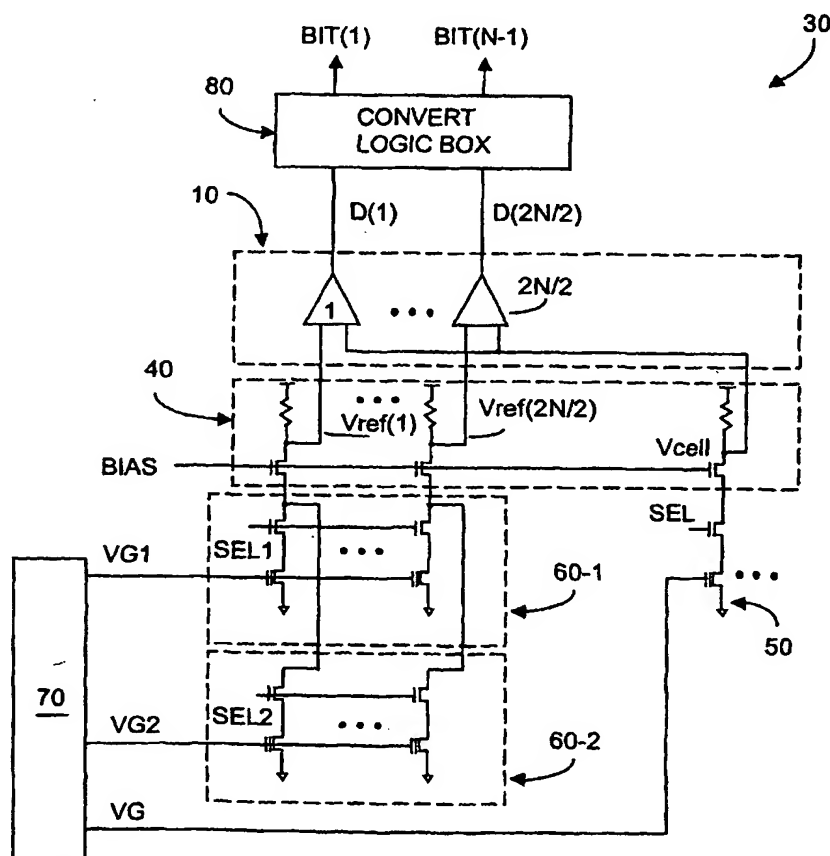
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(54) Title: MULTIPLE LEVEL FLASH MEMORY

(57) Abstract: Data stored in multi-level memory cells (50) is rapidly read out with high resolution by generating and coupling a predetermined and preferable low number of large magnitude jump-like voltage changes to the control gates of the memory cells. The magnitude of the jumps can be a substantial fraction of the power supply level (VDC) and will be many times the Vt levels associated with the memory cells, e.g., the control gate voltage changes in jump-steps from say 4V to 6V to 8V. Use of a low number of jump-steps reduces read out time by permitting read out of a plurality of Vt levels during a given control voltage magnitude. Further, use of large but different magnitude control gate voltages provides good read out resolution over the range of Vt values. Reference cells (601 and 602) are provided to improve tracking, and DRAM type sense amplifiers (10) are provided to maintain high noise immunity.

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MULTIPLE LEVEL FLASH MEMORY

RELATIONSHIP TO PENDING APPLICATIONS

Priority is claimed from U.S. provisional patent application serial number 60/158,325 filed on 8 October 1999 by applicants Lee, Hsu, and Tsao herein,

5   and entitled "Multiple Level Flash Memory".

FIELD OF THE INVENTION

The present invention is directed general to non-volatile memory including so-called multiple-level memory capable of storing more than one data-bit per cell, and more particularly to circuits and techniques for reading date from

10   multiple-level non-volatile memory cells.

BACKGROUND OF THE INVENTION

Historically non-volatile memory such as electrically erasable programmable read-only-memory (EEPROM) or flash memory provided memory cells that were binary, and could store a single bit, e.g., a logical or binary "0" or "1". A

15   typical memory cell is a MOS device that includes source and drain regions formed in a substrate, a floating gate separated from the source, drain, and intermediate region of the substrate by a thin oxide layer, and an overlying control gate separated from the floating gate by a thicker oxide layer.

Coupling appropriate voltage levels to the control gate, source, or drain can

20   cause electrons to collect on the floating gate, where their presence tends to counteract the voltage level on the floating gate, reducing source-drain current flow through the cell. A sense amplifier coupled to the source of the cell can detect the reduced current flow and report a "0" as being stored in the cell. On the other hand, when the cell is erased by coupling appropriate

voltages to the control gate, source, or drain, the floating gate retains minimal charge and control gate potential will turn-on the cell, producing drain-source current flow that the sense amplifier reports as a stored "1".

Discerning whether a memory cell is storing a "0" or "1" is straightforward.

5   But more recently, in an attempt to increase storage density and low storage cost per bit, so-called multi-level EEPROM and flash memory units have been developed in which a memory cell can store more than one-bit of data. In essence the memory cell now stores what may be described as analog values and the multiple-level cell is characterized by an analog voltage

10   threshold value, Vt.   Although multi-level cells and arrays can provide density and cost advantages, it is more difficult to read and identify multiple values stored in a cell, than to read whether the cell is turned off ("0") or on ("1").

Assume a multi-level cell is to store one of sixteen levels. If the analog Vt

15   distribution is from about 1.0 VDC to about 5.5 VDC, the ΔVt value associated with a given storage level is only 300 mV, e.g., (5.5-1.0)/15. Discerning which of the multiple levels has been stored requires accurately and preferably rapidly discerning between ΔVt values that are only 300 mV apart. The requirement to accurately sense with sufficient resolution of at

20   least 300 mV over a range of about 1.0 VDC to about 5.5 VDC can be challenging in practice.

Several solutions have been directed to the problem of reading from multi-level memory cells. For example, U.S. Patent no. 5,508,958 to Fazio, et al. (1996) and U.S. Patent no. 5,751,635 to Wong, et al. (1998) disclose

25   techniques for sensing the state of floating gate memory cells by applying a step-wise increasing variable voltage to the control gate of the memory cells. Fig. 1 herein exemplifies this approach, in which a stepwise-increased voltage (or ramped voltage) is applied to the control gates of cells to alter the

drain-source channel current (Ids)of the cells. The value of Ids will change
st pwise, according to the difference between the nominal Vt valu for the
cell, and the control gate voltage at the moment.

In Fazio '958 and Wong '635 configurations, sensing DIDS involves coupling
5   a fixed reference current loading to the drain node of the memory cell, to form
a ratio-type sense amplifier.   When control gate voltage is less than Vt for a
cell, Ids for that cell will be less than a pre-selected reference current, which
causes the sense amplifier output to be "1".   This sense amplifier reading
indicates that the control gate voltage should be further increased, until a
10   predetermined value exceeding the cell Vt is attained. When the control gate
ramp voltage level exceeds the cell Vt, Ids will exceed the reference current,
which pulls the sense amplifier output low, which allows the value of the cell
data to be determined.

Fig. 2 is an exemplary graph of Ids distribution for a multi-level memory cell
15   having sixteen levels of analog Vt values ranging from Vt1 = 1 V to Vt16 = 7.5
V, when applying drain voltage of 1 V and sweeping the control gate voltage
VG. In Fazio-Wong systems, the sense amplifier output is almost digital in
that large voltage swings occur. If there are sixteen Vt levels ranging from
about 1 VDC to about 7.5 VDC, the ΔVt per storage level will be on the range
20   of about 0.5 V. Referring to Fig. 2, assume that the reference current is
selected as 40 µA. The horizontal row of black dots in Fig. 2 represents the
sixteen gate voltages required to read out the respective sixteen levels of Vt
for the memory cell. Note that since cell current Ids is compared with a fixed
reference current using a ramp-like gate voltage, a linear current difference
25   between adjacent Vt levels can be maintained, along with a reasonable
operating margin. Thus, Fazio-Wong type read out can offer advantages
including improved read out resolution, and higher sense amplifier noise
immunity margin. Typically a Fazio-Wong type system can implement
perhaps thirty-two to one-hundred fifty-six levels of Vt per memory cell.

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However, a significant drawback of the Fazio-Wong type sense scheme is the requirement for very accurate control gate voltage levels. For each ramp step, the control gate voltage must remain at a voltage level sufficiently long

5   to attain a stable magnitude. Unfortunately this requirement decreases operating speed for the memory system, especially read access time. For a multi-level cell storing a large number of levels, i.e., 256 levels, read time can become excessive. As a result, the Fazio-Wong type approach shown in Figs. 1 and 2 is best suited to low-speed operations, such as the storage and

10   playback for speech data.

Further, the long read process required in a Fazio-Wong type system increases the memory cell's exposure to stress. Typically read out operations for multi-level cells requires larger magnitude control gate voltage than for binary storage cells. As a result, as long as the control gate voltage

15   is applied to a row, or word line in an array of memory cells, all cells on the row will experience stress from the large magnitude gate voltage, and can experience a shift in cell Vt value. Therefore, it is desired to reduce read time, to reduce exposure to stress and possible disturbance of cell Vt values.

In an attempt to overcome the above-mentioned slow speed problems,

20   alternative sensing methods have been developed, for example as disclosed in U.S. Patent no. 5,838,612 to Calligaro et al., and U.S. Patent no. 5,220,531 to Blythe et al. Rather than use Fazio-Wong type low-speed, stepwise increased gate voltages, in systems according to Calligaro-Blythe, a fixed gate voltage is coupled directly applied to the control gate of the memory cell.

25   The fixed-gate voltage causes memory cells having different values of Vt to conduct different magnitudes of cell Ids drain-source channel current. In Calligaro-Blythe type systems, the memory cell drain is connected to a reference current load, such as was described above with respect to Fazio-

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Wong. A differential output voltage is derived from the ratio between the cell Ids current and the reference current.

But the Calliagaro-Blythe approach has a significant drawback arising from the basic characteristic of MOS devices. In a MOS memory cell, the channel

5　current distribution for each Vt level is not linear, but rather tends to saturate as gate voltage increases relative to magnitude of Vt for the cell. Fig. 3 depicts cell current Ids for sixteen values of Vt (Vt1, Vt2, ... Vt15, Vt16) for a fixed gate voltage, e.g., VG = 8 VDC that is sufficiently high to turn-on all cells in the sixteen Vt range. Current distribution clearly is not linear. There

10　is better current resolution in the high Vt range, but very poor resolution in the low Vt range. This phenomenon makes it very difficult to store a large number of Vt levels in a multi-level cell because resolution will be lost for the lower Vt values. Thus, the Calliagaro-Blythe approach is best used for storing a low number of Vt levels, such as four or eight levels per memory

15　cell.

There is a need for a read out system and method for use with multi-level memory cells, in which read out can occur relatively rapidly, while maintaining acceptable read out resolution over a range of Vt levels. Such system and method preferably should be implementable inexpensively and using existing

20　processing techniques.

The present invention provides such a system and method.

SUMMARY OF THE INVENTION

The present invention reads out data stored in multi-level memory cells by generating and coupling a predetermined and preferably low number of large

25　magnitude jump-like voltage changes to the control gates of the memory cells. The magnitude of the jumps can be a substantial fraction of the power supply level and will be many times the ΔVt levels associated with the

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memory cells. For example, a first control gate voltage of perhaps 4 V is coupled to the multi-level cells, then the control gate voltage jumps to perhaps 6 V, then to 8 V, rather than slowly incr ase step-wise as in the prior art. The use of a relatively low number (e.g., two, three, etc.) of large

5   magnitude step control gate voltages (e.g., 4 V, 6 V, 8 V) substantially reduces read out time by permitting read out of a plurality of Vt levels during a given control voltage magnitude. Further, the use of large but different magnitude control gate voltages provides good read out resolution over the range of Vt values. The present invention further includes reference cells

10   that help improve tracking against variation in fabrication process, power supply, and temperature. Further, the present invention preferably uses high sensitivity, high noise immunity DRAM-type sense amplifiers to further improve read out performance.

Other features and advantages of the invention will appear from the following
15   description in which the preferred embodiments have been set forth in detail, in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 depicts a system for reading data from multi-level memory cells, according to the prior art;

20   FIG. 2 is depicts distribution of channel current (Ids) versus gate voltage (VG) for a multi-level memory cell, and shows various Vt values for a given value of Ids as used in Fazio-Wong type read-out systems, according to the prior art;

FIG. 3 depicts (computer simulated) distribution of channel current (Ids)
25   versus gate voltage (VG) for a multi-level memory cell, and shows loss of Ids resolution at a given value of VG as memory cell saturation occurs, as used in Calligaro-Blythe type read-out systems, according to the prior art;

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FIG. 4 depicts (computer-simulated) distribution of channel current (Ids) versus gate voltage (VG) for a multi-level memory cell, and shows preservation of substantially linear Ids resolution for lower and for higher values of Vt, as used in a read-out system, according to the present

5   invention;

FIG. 5 depicts (computer-simulated) distribution of channel current (Ids) versus gate voltage (VG) for a multi-level memory cell, and shows preservation of substantially linear Ids resolution for lower, for intermediate, and for higher values of Vt, as used in a read-out system, according to the

10   present invention;

FIG. 6A depicts a preferred embodiment of a DRAM-type sense amplifier used to read-out muli-level memory cells, according to the present invention;

FIGS. 6B-6B depict waveforms present at various nodes in the DRAM-sense amplifier shown in Fig. 6A, according to the present invention; and

15   FIG. 7 is an exemplary block diagram of a multi-level cell memory system with high voltage-step read-out, according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

As noted, in the prior art according to Fazio-Wong, multi-level memory cells are read out using control gate voltages that increase stepwise using a large

20   number of steps separated from each other by small voltage increments. The magnitude of these increments (e.g., hundreds of mV or less) is on the order of memory cell threshold voltages, and is a small fraction (perhaps 10% or less) of the operating potential (perhaps 10 V). If the time delays associated with providing, say, 256 stable voltage levels for a multi-level memory cell

25   having 256 Vt values are reduced by using a single fixed control gate potential, read out resolution is substantially diminished.

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In contrast to the above techniques, the present invention reads out multi-level memory cells by generating and coupling a predetermined and preferably low number of large magnitude jump-like voltage changes to the control gates of the memory cells. The magnitude of the jumps can be a

5   substantial fraction of the power supply level and will be many times the ΔVt levels associated with the memory cells.

Referring now to Fig. 4, in one embodiment the number of large magnitude jump-like changes in the control gate voltage (VG) is two, and the magnitude of the two VG levels is 4 V and 8 V. Assume that the memory cells in

10   questions that are to be read out have sixteen values of Vt: Vt1, Vt2, ... Vt15, Vt16. In the left hand portion of Fig. 4, when VG = 4 V, the lower level threshold values (here Vt1, Vt2, ... Vt7, Vt8) may be read out. Next the VG level jumps from 4 V to 6 V, and when VG = 8 V, the higher level threshold values (here Vt9, Vt10, ... Vt15, Vt16) may be read out.

15   Note that in each case, when VG = 4 V or when VG = 8 V, there is substantial Ids (or I_{CELL}) linearity, e.g., read out resolution will be high throughout the Vt range. This is an improvement over the non-linear, resolution loss problems associated with Calligaro-Blythe type methods.

For example when VG = 4 V, memory cells associated with lower Vt values

20   (e.g., Vt1, Vt2 ... Vt7, Vt8) will turn on, and Ids current flow through these memory cells will be quite linear and will provide better resolution than when VG is at a higher magnitude, for example as high as VG = 8 V. Of course at the lower level of VG, e.g., VG = 4 V, memory cells characterized by higher value Vt (e.g., Vt9 ... Vt16) are not turned on and will conduct essentially no

25   Ids current. (Such higher level Vt cells would exhibit poor read out resolution if attempted at VG = 4 V). But at the higher level VG = 8 V, all the memory cells will turn on since VG > Vt, whereupon memory cells associated with higher Vt (e.g., Vt9 ... Vt16) conduct Ids in a linear fashion, as shown by Fig.

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4. High resolution read out from these higher Vt cells thus takes place when VG = 8 V, e.g., when VG is a magnitude sufficiently high to turn on the highest Vt memory cell, which is to say, to turn-on all Vt memory cells. Understandably, when VG = 8 V, read out resolution of the lower Vt cells

5 (e.g., Vt1.... Vt8) will diminish as these cells will saturate and be in a non-linear regime. But by applying the lower VG = 4 V and reading out the lower Vt memory cells, and then applying the higher VG = 8 V and reading out the higher Vt memory cells, high resolution read out is obtained from all cells. Thus, while use of a single fixed VG will not provide high resolution read out

10 at all Vt levels, the use of several (e.g., perhaps two to four) jump-steps of high voltage VG can permit reading out all multi-level cells rapidly and with high resolution.

In Fig. 4, even through sixteen levels of Vt are present, there is no necessity to generate sixteen levels of VG, in which level that might otherwise have to

15 be generated, at least according to the prior art, would be typically a few hundred mV separated from an adjacent level. Note too, there is no need to wait for each of sixteen stair-stepped voltage levels to stabilize before attempting read out, as in the prior art. Instead, if two jump-steps are used in the present invention, as shown in Fig. 4, the time improvement in reading

20 out sixteen level Vt multi-level cells will be eight-fold compared to a Fazio-Wong type system. If four jump-steps were used in the present invention, the time improvement over a Fazio-Wong type system would be four-fold. However the time improvement realized by the present invention increases substantially as the number of Vt levels is increased. Thus, for a memory

25 array comprising a plurality of 256 Vt level multi-level memory cells, the time advantage over a Fazio-Wong system would be 128 if two jump-steps were used in the present invention, and would be 64 if four jump-steps were used.

At each magnitude of the jump-step VG voltage, multiple levels of Vt read outs occur simultaneously, e.g., Vt1 through Vt8 levels when VG = 4 V, and

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Vt 9 through Vt16 when VG = 8 V for the embodim nt depicted by Fig. 4. It is seen that Vt-groups of memory cells may be defined, e.g., a lower Vt range of Vt1 .. Vt8, and a higher Vt range of Vt9 ... Vt16, as exemplified by Fig. 4. Read out of the lower Vt range of memory cells occurs during application of

5   the lower VG voltage, e.g., VG = 4 V in Fig. 4, and read out of the higher Vt range occurs during application of the higher VG voltage, e.g., VG = 8 V in Fig. 4.

In addition to providing a high speed, high resolution method of reading out multi-level memory cells, sensing according to the present invention can in

10   essence extend the Vt range. Assume for example that twenty-four Vt levels are to be defined, rather than the sixteen Vt levels used in Fig. 4. Thus, a low Vt level group (Vt1 ... Vt8) may defined having cell Vt values from say 1 V to 3.1 V. A middle Vt level group (Vt9 ... Vt16) may be defined having Vt values from say 3.4 V to 5.5 V, and a high Vt level group (Vt17 ... Vgt24) may be

15   defined having Vt values from say 5.8 V to 7.9 V. In this twenty-four Vt level example, ΔVt is about 0.3 V.

Fig. 5 depicts Ids current versus VG for an embodiment having twenty-four Vt levels, where the number of jump-steps is three, and the VG voltage coupled to the control gates of the multi-level memory cells is 4 V, then 6 V, then 8 V,

20   although for the specific Vt voltages enumerated above, jump-step magnitudes might be 4 V, 6.5 V, and 9 V. Understandably, more than three jump-steps could be provided, if desired.

In the embodiment shown in Fig. 5, at VG = 4 V, the lower Vt level cells (e.g., Vt1, Vt2, ... Vt7, Vt8) conduct current in a substantially linear regime and may

25   now be read out, but the higher level cells (e.g., Vt9 ... Vt 24) do not yet conduct current. VG is then jumped from 4 V to 6 V, whereupon memory cells having middle range Vt (Vt9, Vt10, ... Vt15, Vt16) conduct current in a linear regime and may now be read out. Of course the lower level Vt cells also

conduct, but in a non-linear regime, and the higher level Vt cells (Vt17, Vt18, ... Vt23, Vt24 do not yet conduct current. VG is next jumped to 8 V whereupon the higher level Vt cells (Vt17 .. Vt24) conduct current in a linear regime and may now be read out. Since VG is now greater than Vt for all of

5   the memory cells, cells characterized by Vt1, Vt2, ... Vt15, Vt16 also conduct current, but in a non-linear regime.

The number of jump-steps, e.g., two in Fig. 4, three in Fig. 5, etc., and the magnitudes of the large jump-step voltages, e.g., 4 V, 6 V, 8 V, etc. will be designed into the system depending upon the resolution and read out time

10   that is required. Increasing the number of jump-steps can, if the number of steps is made very large, contribute to memory cell stress.

The present invention further includes reference cells that help improve tracking against variation in fabrication process, power supply, and temperature. Further, the present invention preferably uses high sensitivity,

15   high noise immunity DRAM-type sense amplifiers to further improve read out performance.

In the preferred embodiment, the VG gate voltage is simultanously applied to the reference cells (e.g., 16 such cells in an appropriate embodiment) and to the multi-level memory cells. In another embodiment, the multiple reference

20   cells are divided into groups, e.g., two groups, wherein a first group includes lower value Vt cells, and a second group includes higher Vt cells. When reading out, the lower magnitude gate voltage is applied to the first group to achieve high read out resolution among the lower Vt level memory cells. Meanwhile, the higher gate voltage is applied to the second group to achieve

25   high resolution in the higher Vt level memory cells.

Figs. 6A-6 and Fig. 7 depict exemplary systems to implement the present invention. It is first noted that while using a preferably small number of large magnitude jump-steps can provide rapid and high resolution read out of multi-level memory cells, the read out sense amplifier can diminish the overall

5 effective read out resolution. For example, ratio-type sense amplifiers as shown in prior art Fig. 1 compare cell current with a reference current (generated by a NMOS device, a PMOS device, a resistor, or any other current loading) and transfer the ratio of cell current and reference current into an analog voltage output. For multi-level memory cells, the cell current

10 difference between levels can be very small, and the differential voltage to be read out with a sense amplifier can also be very small, perhaps 10 mV. This small differential voltage requires a sense amplifier having high sensitivity but also high noise-immunity to detect. But conventional differential-type ratio sense amplifiers as used in the prior art are not good candidates in a high

15 resolution system due to the poor noise-immunity exhibited by such sense amplifiers.

In a preferred embodiment, as a substitute for prior art differential-type sense amplifiers, the invention provides a DRAM-type sense amplifier 10, such as shown in Fig. 6A to sense Ids current flow in multi-level memory cells.

20 Advantageously, DRAM-type sense amplifier 10 uses a two-phase, sampling-and-evaluation operation. Referring to Figs. 6A-6F, during the sampling phase defined by a Sample Enable signal (see Figs. 6B, 6C) DRAM-type sense amplifier 10 samples an input voltage (V_{CELL}) and samples a reference voltage (V_{REF}) from data lines to a sensing node (DATA and its complement

25 DATAB, see Fig. 6F in which Vref is shown in bold for clarity).

During an evaluation phase, sense amplifier 10 isolates the sensing nodes from the data lines, and a cross-coupled latch circuit 20 is activated to develop the differential input voltages into a full Vdd-Vss range. This mode of operation assures higher noise-immunity than prior art sense amplifiers.

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For example, prior art differential-type sense amplifiers do not latch or de-
couple th input voltage from the s nsing nodes, thus putting the sense
amplifier into a high-gain regime all the time. This prior art high-gain regime
operation makes it difficult to maintain a stable and accurate output during

5   the entire, typically noisy, sensing process. In addition to advantageously de-
coupling the input voltage from the sense nodes, DRAM-type sense amplifier
10 provides very high sensitivity, e.g., voltage levels in the few mV range can
be sensed. Thus, the present invention preferably employs a DRAM-type
sense amplifier to sense multi-level memory cells.

10   Fig. 7 is an exemplary block diagram for a system 30 implementing the
present invention. System 30 includes a plurality of DRAM-type sense
amplifiers 10, for example such as was described with reference to Figs. 6A-
6F, a plurality of ratio-type sense amplifier 40, the multi-level memory cells 50 –
(only one of an array of the cells being shown for clarity), a first reference

15   group of multi-level memory cells 60-1, a second reference group of multi-
level memory cells 60-2, a gate voltage generator 70, and a convert logic box
unit 80. Each DRAM-type sense amplifier 10 receives a first input from the
selected memory cell, and a second input from one of the reference cells.
Converter logic unit 80 receive outputs from the sense amplifiers and
20   converts the outputs into digital data, e.g., BIT(1), etc.

The multi-level memory cells preferably are divided into several groups, such
as group (a) to group (h), with a plurality of multi-level memory cells in each
group. The Vt for cells in each group is incremental, as was described earlier
herein. Gate voltage generator 70 generates the jump-step voltages VG
25   coupled to the gates of selected memory cells, and also to the gates of
reference cells.

Assume read operation will now take place. Assume also that 2^N levels of Vt
are stored in a multi-level memory cell, and that there are 2^N reference cells

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divided into two groups G1 (60-1) and G2 (60-2) with $2^N/2$ reference cells in
ach group. Gate voltage generator 70 will first output a first gate voltage
VG1 to the first reference cells in group G1 (60-1) and to the selected
memory cell. As shown in Fig. 7, the drain of the reference cells and of the
5   memory cell are connected to ratio-type sense amplifiers 40, which convert
the currents of each reference cell and the memory cell current into $2^N/2$
reference voltages Vref $_{(1)}$ to Vref $_{(2N/2)}$ and into cell voltage Vcell.

Block 10 includes $2^N/2$ DRAM-type sense amplifiers, and each sense
amplifier receives and compares Vcell with one of the reference voltage, Vref
10    $_{(1)}$ to Vref $_{(2N/2)}$, and then generates the comparison results, $D_{(1)}$ to $D_{(2N/2)}$. The
logic block then receives and converts the results $D_{(1)}$ to $D_{(2N/2)}$ into N-1 bit
digital data. If a memory cell's Vt does not belong to the first group of
reference cells this can be noticed from the N-1 bit data, and Gate Voltage
Generator 70 will generate a second gate voltage, VG2 to the second
15   reference cells group G2 (60-2) and to the selected cell. Then, the read
process of comparing currents of the selected cell with that of the $2^N/2$
reference cells in the second group as above-described is repeated, to
determine the memory cell's N-1 bit data. Thus, only two jump-steps of gate
voltage are needed to read the multi-level memory cell. Note too that this
20   described method of sensing can be used to implement parallel sensing
wherein the above-described two jump-step gate voltage is applied to more
than one selected memory cell. The configuration noted in Fig. 7 would be
increased as needed to implement a parallel read operation.

Modifications and variations may be made to the disclosed embodiments
25   without departing from the subject and spirit of the invention as defined by the
following claims.

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CLAIMS

1. A method of reading out data from a plurality of multi-level memory cells characterizable by a plurality of Vt levels, the method comprising the following steps:

5   (a) coupling to a control gate of said multi-level memory cells a jump-step voltage gate signal having a first magnitude level and a higher second magnitude separated from said first magnitude level by at least one volt;

     (b) when said voltage gate signal is at said first magnitude level, reading out from said multi-level memory cells current levels associated with 10 ones of said cells characterized by lower magnitude levels of said Vt levels; and

     (c) when said voltage gate signal is at said second magnitude level, reading out from said multi-level memory cells current levels associated with ones of said cells characterized by higher magnitude levels of said Vt levels.

15   2. The method of claim 1, wherein said first magnitude level and said second magnitude level of said voltage gate signal are separated by at least two volts.

3. The method of claim 1, wherein said first magnitude level and said second magnitude level of said voltage gate signal are separated by at least 20 three volts.

4. The method of claim 1, wherein step (b) and step (c) is carried out at least in part using a DRAM-type sense amplifier.

5. The method of claim 1, further including divided said cells into at least three groups definable as a first block of said cells associated with a 25 lower range of said Vt levels, a second block of units associated with a middle range of said Vt levels, and a third block of units associated with a higher range of said Vt levels.

6.   The method of claim 1, wherein a number of said Vt levels exceeds a value selected from a group consisting of (i) four, (ii) sixteen, (iii) thirty-two, (iv) sixty-four, (v) one-hundred twenty-eight, (vi) two-hundred fifty-six, and (vii) five hundred twelve.

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7.   The method of claim 1, further including providing a plurality of reference memory cells characterizable by a plurality of Vt values, and divisible into groups according to blocks of said Vt values.

8. A system to read out out data from a plurality of multi-level memory
10   cells characterizable by a plurality of Vt levels, the system comprising:

a voltage generator outputting a jump-step voltage gate signal having a first magnitude level and a higher second magnitude separated from said first magnitude level by at least one volt, said jump-step voltage gate signal being coupled to control gates of said cells; and
15   means for reading out from said multi-level memory cells current levels associated with ones of said cells characterized by lower magnitude levels of said Vt levels when said voltage gate signal is at said first magnitude level,; and for readout of from said multi-level memory cells current levels associated with ones of said cells characterized by higher magnitude levels
20   of said Vt levels when said voltage gate signal is at said second magnitude level.

9. The system of claim 10, wherein said first magnitude level and said second magnitude level of said voltage gate signal are separated by at least two volts.

25   10.   The system of claim 10, wherein said first magnitude level and said second magnitude level of said voltage gate signal are separated by at least three volts.

11.   The system of claim 10, wherein said means for reading out includ s a DRAM-type sense amplifi r.

12.   The system of claim 10, wherein said cells are divided into at least three groups definable as a first block of said cells associated with a
5   lower range of said Vt levels, a second block of units associated with a middle range of said Vt levels, and a third block of units associated with a higher range of said Vt levels.

13.   The system of claim 10, wherein a number of said Vt levels exceeds a value selected from a group consisting of (i) four, (ii) sixteen, (iii)
10   thirty-two, (iv) sixty-four, (v) one-hundred twenty-eight, (vi) two-hundred fifty-six, and (vii) five hundred twelve.

14.   The system of claim 10, further including a plurality of reference memory cells characterizable by a plurality of Vt values, and divisible into
15   groups according to blocks of said Vt values.

15.   The system of claim 10, further including means for compensating for at least one of (a) variation in fabrication process, (b) power supply magnitude coupled to said system, and (c) temperature of said system.
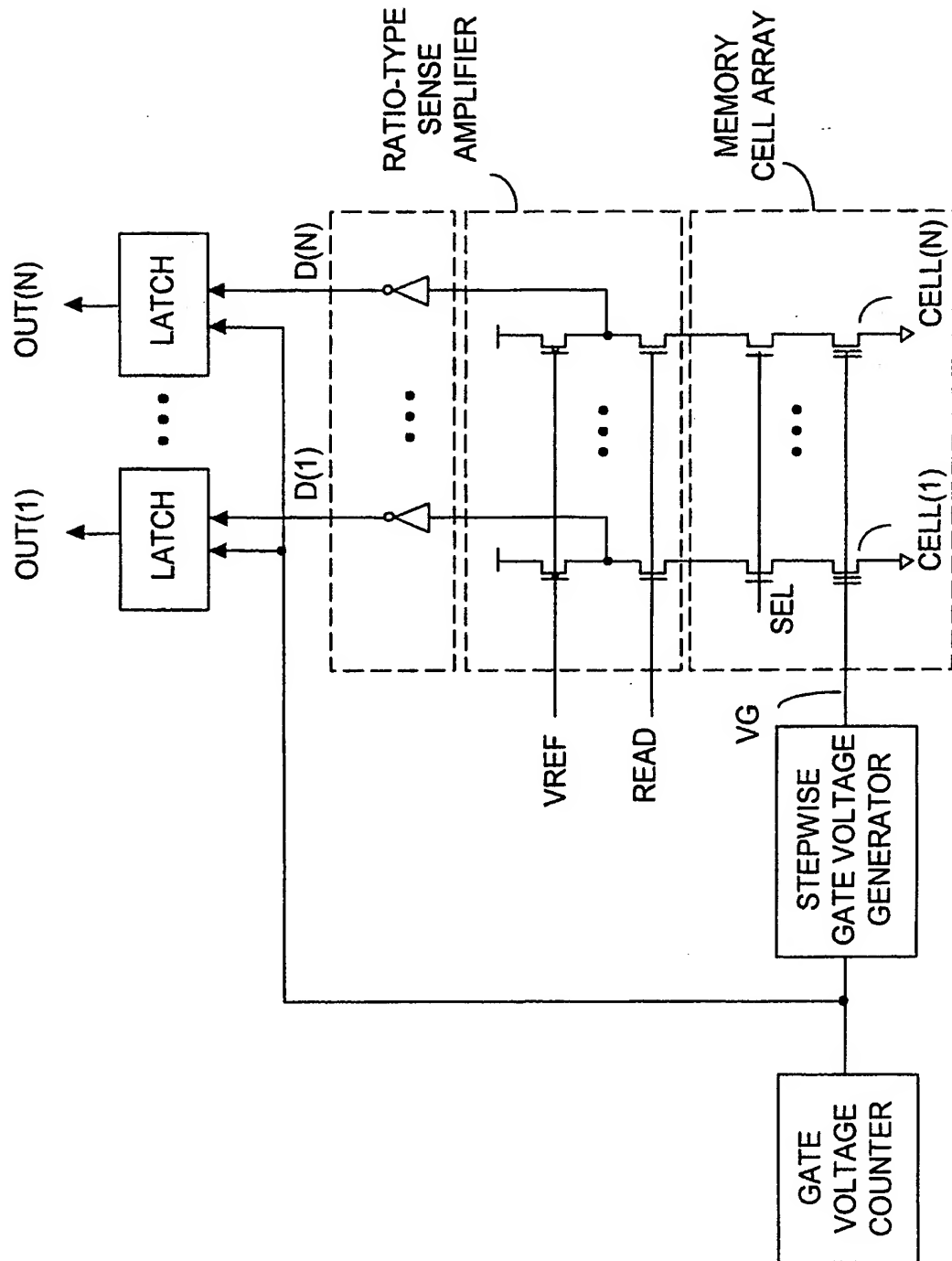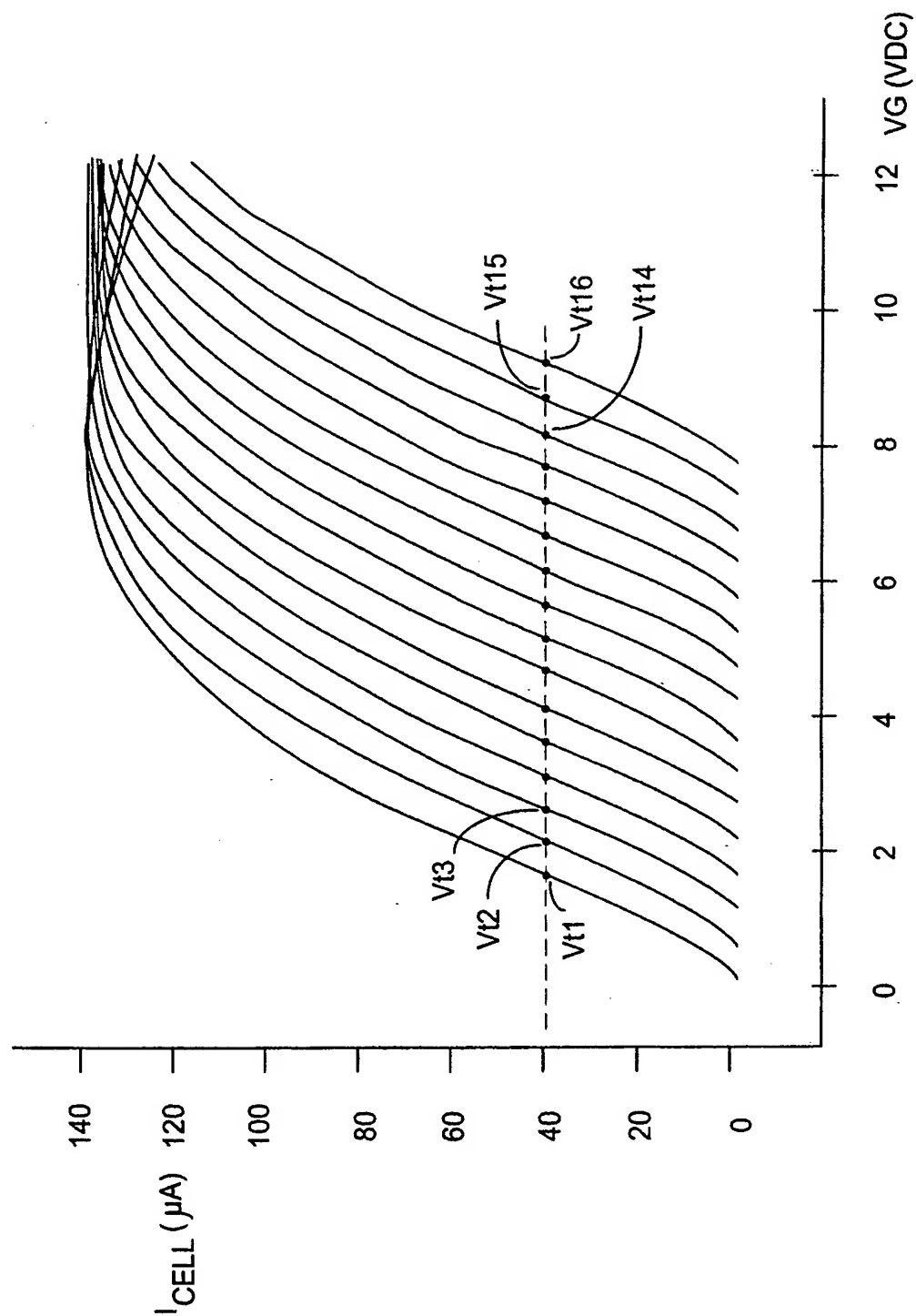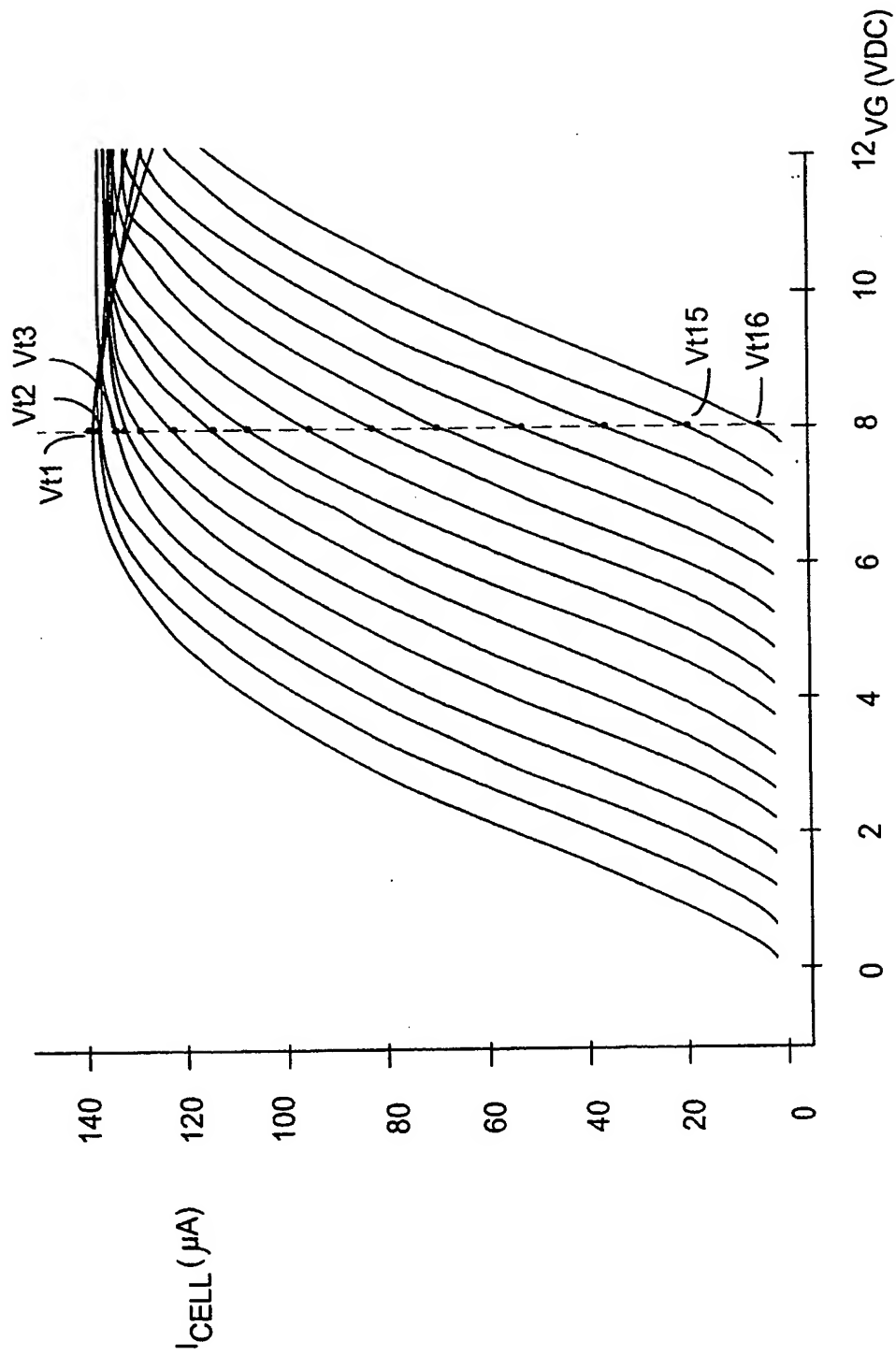
17

FIG. 1 (PRIOR ART)

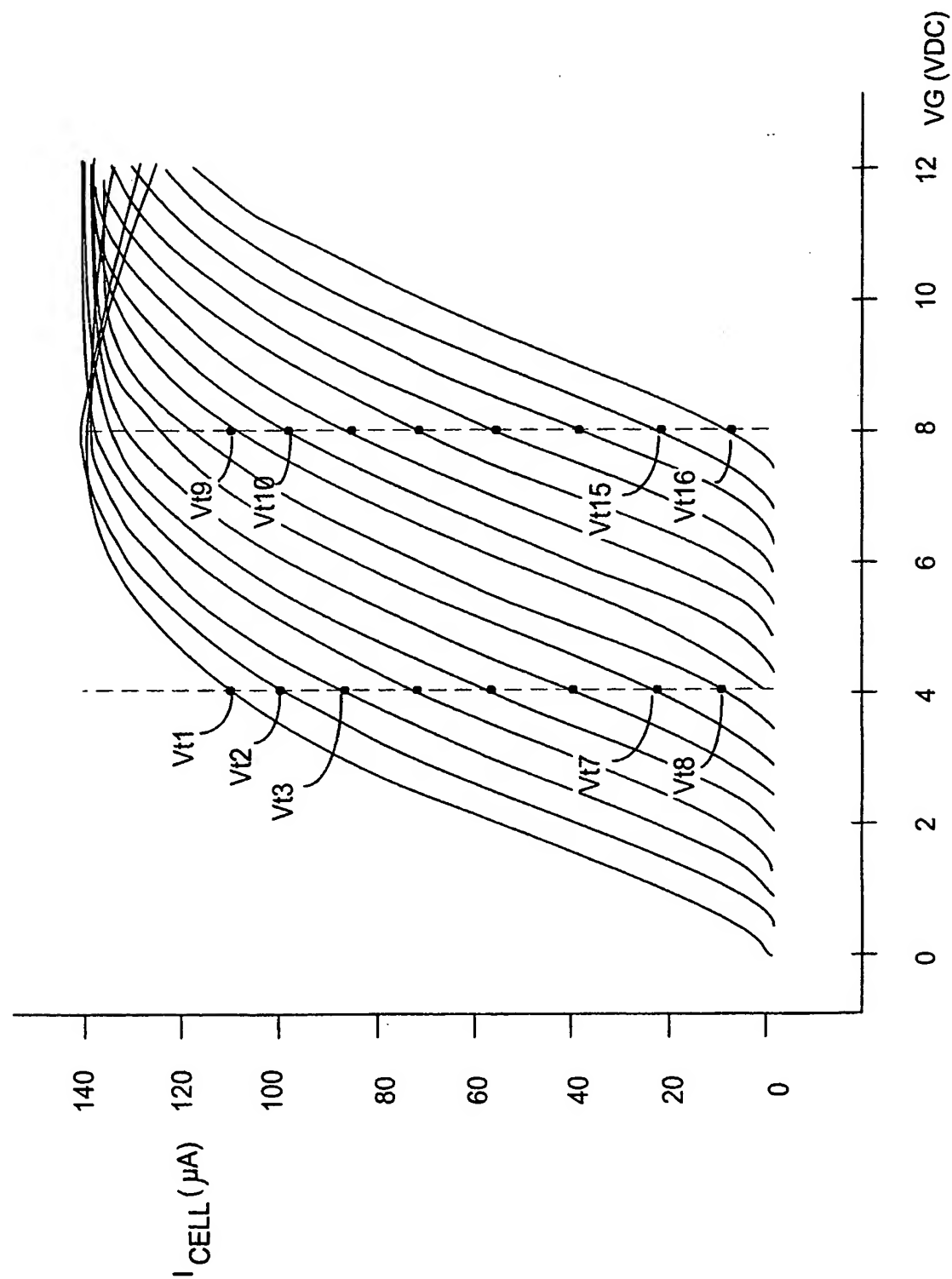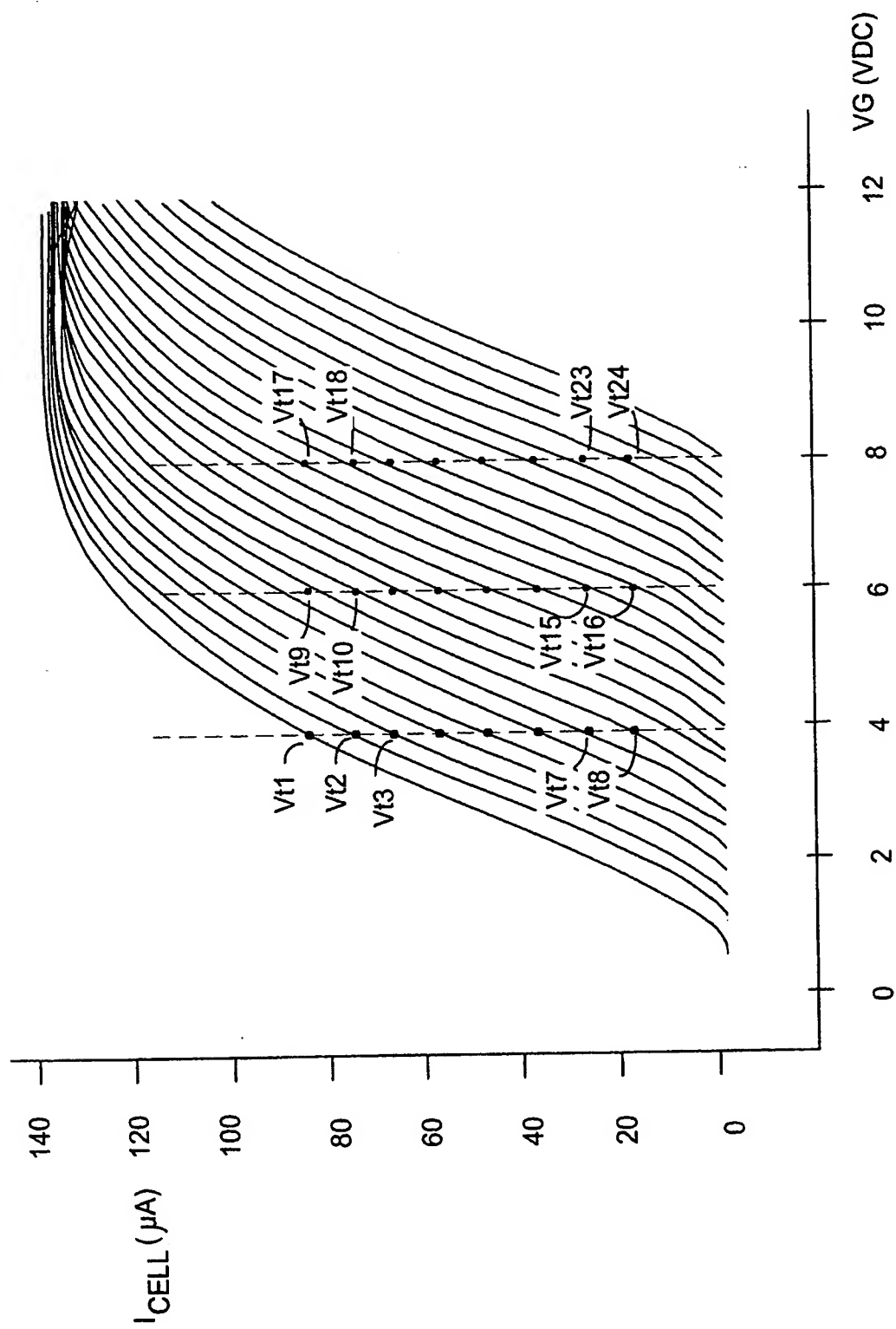FIG. 2 (PRIOR ART)

FIG. 3 (PRIOR ART)

FIG. 4

FIG. 5
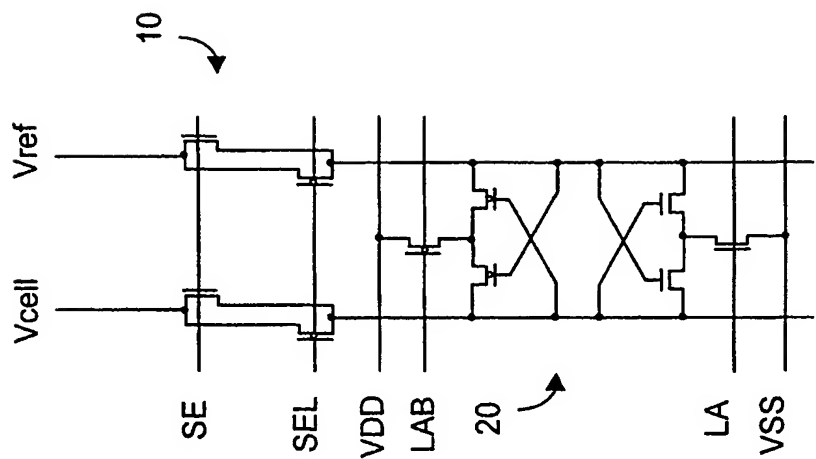
FIG. 6B

FIG. 6C

FIG. 6D

FIG. 6E

FIG. 6F

SE

SEB

LA

LAB

DATA

DATAB

Vref

LAST DATA

NEW DATA
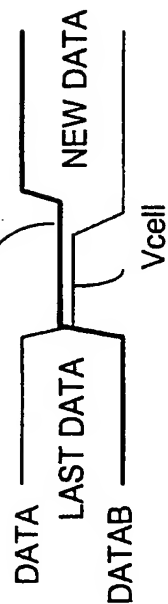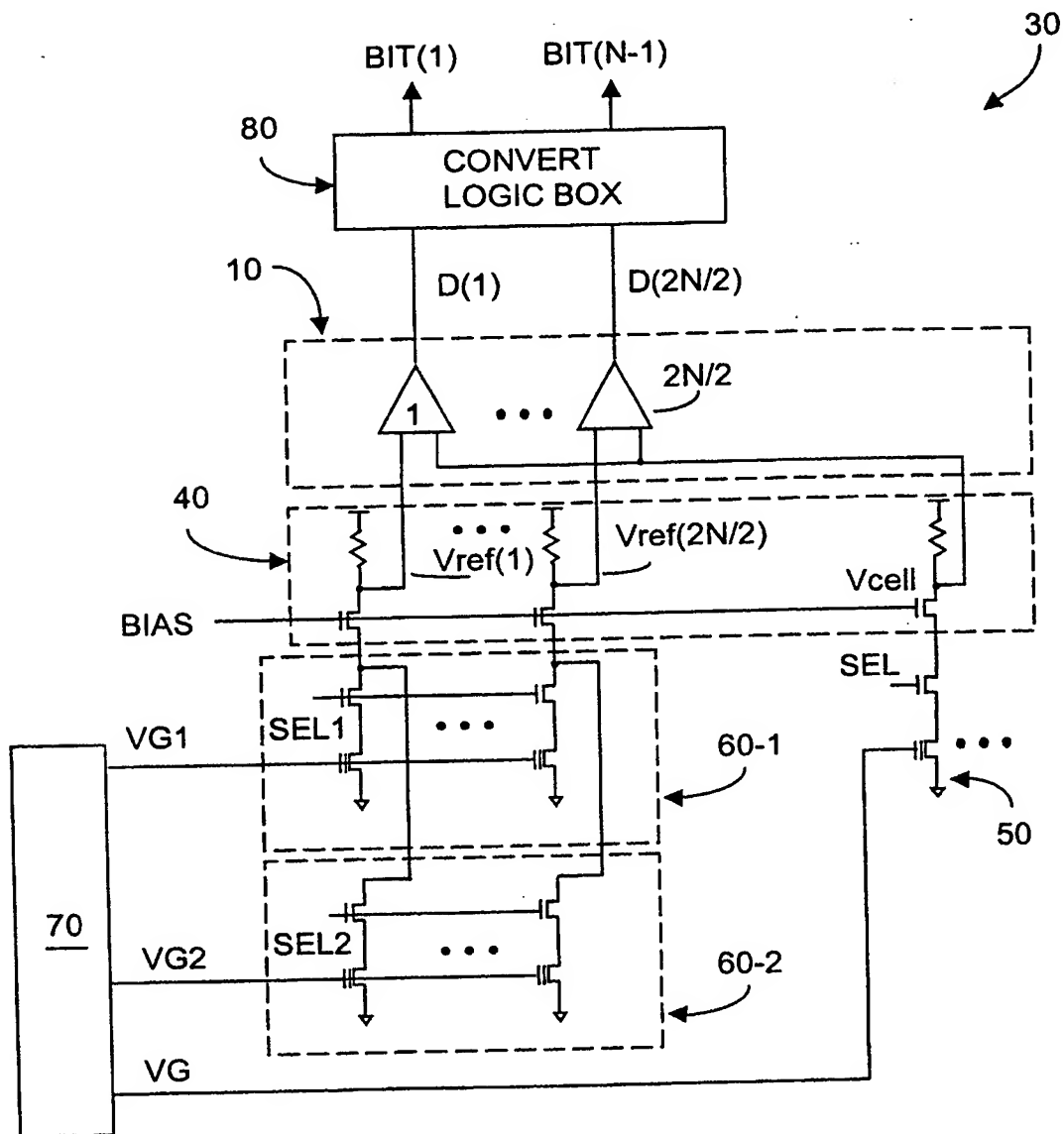
Vcell

FIG. 6A

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/27755

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :G11C 16/04, 16/06
US CL :365/185.03, 185.11, 185.18, 185.19, 185.2

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/185.03, 185.11, 185.18, 185.19, 185.2

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,790,454 A (CHOI) 04 August 1998 (04.08.1998), col. 7, line 43 to col. 9, line 38, FIGS. 6-8	1, 2, 3, 6, 8
Y		4, 7
A		5
Y	US 5,936,906 A (TSEN) 10 August 1999 (10.08.1999), Fig. 2.	4, 7

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 DECEMBER 2000	17 JAN 2001

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	VANTHU NGUYEN
Facsimile No. (703) 305-3230	Telephone No. (703) 308-0956

Form PCT/ISA/210 (second sheet) (July 1998)★

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US00/27755

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
   because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
   because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 9-15
   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest ☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

Form PCT/ISA.210 (continuation of first sheet(1)) (July 1998)∗